12 GHz Low-Noise MMIC Amplifier Designed with a Noise Model that Scales with MODFET Size and Bias

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***Abstract*— A scalable, bias-dependent FET noise model was developed for MMIC design. A three-stage, 12 GHz, MMIC, low-noise amplifier (LNA) was designed with the model. The LNA has a 1.6 dB noise figure and 25.6 dB gain. Lumped elements were used to design an LNA that was significantly smaller per stage (0.31 mm^2) than previous MMIC LNAs**

I. Introduction

MMICs are gradually replacing hybrid MICs in commercial applications. Downconverters for 12 GHz direct broadcast satellite (DBS) receivers have found wide acceptance [1]. However, the LNA of most 12 GHz DBS receivers is still a hybrid MIC. Successful replacement of hybrid MICs with MMICs requires similar or better performance and reliability with higher manufacturability and lower cost. This paper describes a design that addresses manufacturability and cost via small chip size. The DBS application is so large and well known it is an ideal vehicle for comparing circuit performance and design techniques.

Another market for MMICs is custom ICs. Speed to market and the cost of engineering design are important for these markets. Success on the first design iteration is key. This requires accurate computer aided design models. This paper describes a noise model that was developed for MMIC design. The noise model scales with FET size and FET bias. The model was used successfully to design the 12 GHz LNA.

II. MMIC Technology

This MMIC process was developed for high performance instrument applications, such as broad band power amplifiers [2, 3]. However, the process is useful for a variety of applications [4]. The active devices are modified 25 % In pseudomorphic MODFETs, with e-beam written, 0.25 μm, Ti/Pt/Au, mushroom gates [5]. The PMODFETs typically have a maximum f_T greater than 70 GHz, I_{Dmax} of 520 mA/mm and V_{Bgdo} of -11 volts (1 mA/mm). The process has respectable power and noise performance: maximum output power is 700 mW/mm at 40 GHz and F_{min} is 0.8 dB with G_a of 13 dB at 12 GHz. The process uses tantalum nitride thin film resistors, (22 Ω/), bulk resistors, (220 Ω/), silicon nitride MIM capacitors (0.60 pF/μm^2), two levels of interconnect metal and 40x40 μm backside vias (27 pH) [4]. Critical parameters are controlled to better than 16 %. The PMODFETs are reliable with a MTTF greater than 10^6 hours at a channel temperature of 150° C. The process was used to fabricate 2-50 GHz TWAs with 9 dB gain and 20 dBm output power [6].

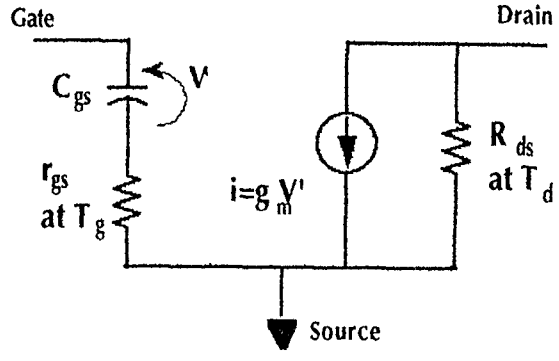

Fig. 1. Noise model for an intrinsic FET.

III. FET Noise Model

The FET noise model developed is based on the noise temperature model of Pospieszalski [7]. The noise sources are thermal noise from the input resistor, r_{gs}, and the parasitic resistors at ambient temperature, T_g, and from the output resistor, R_{ds}, at temperature T_d. The noise model of the intrinsic FET is shown in Fig. 1. T_d is typically 2000 K for a FET biased for lowest F_{min}. T_d is extracted directly from measured noise data and the FET circuit model. The model is not applicable where noise from gate-source leakage current and 1/f noise are significant. The model was implemented into a bias dependent FET model in HP Microwave Design System [11]. This model accurately predicts all four noise parameters as function of frequency using a single modeling parameter: the noise temperature of the output resistor, T_d [7, 8, 9]. Excellent agreement between measured and modeled F_{min} and G_a are shown in Fig. 2. Fig. 3 demonstrates the agreement between measured and modeled S_{11}, S_{22}, and Γ_{opt} (generator reflection coefficient for minimum noise figure).

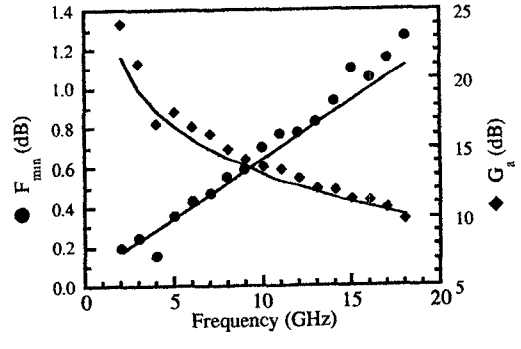

Fig. 2. Plot of measured and modeled F_{min} and G_a versus frequency for a 180 μm wide PMODFET biased at I_{ds} of 60 mA/mm and V_{ds} of 2 V.

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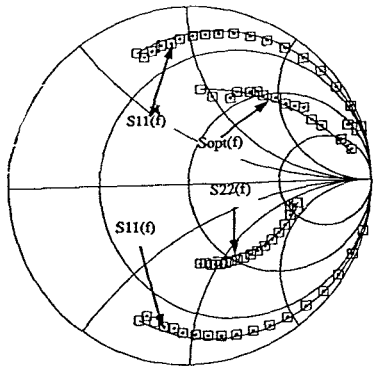

Fig. 3. Smith chart plot of measured and modeled Γ_{opt}, S_{11}, S_{22}, and S_{11}^* versus frequency (2 to 18 GHz) for a 180 μm wide PMODFET biased at I_{ds} of 60 mA/mm and V_{ds} of 2 V.

A noise model that scales with width is essential for MMIC design because FETs of different widths are used and width is optimized in circuit design. The noise model scales with FET size because T_d is a very weak function of width. For example, the normalized extrinsic input resistance, R_{in}, and the normalized optimum generator resistance, R_{opt}, are weak functions of the number of fingers, as shown in Fig. 4 for FETs with fingers 30 and 45 μm wide. However, normalized R_{in} and R_{opt} increase with finger width as expected because normalized gate resistance increases in proportion to gate width.

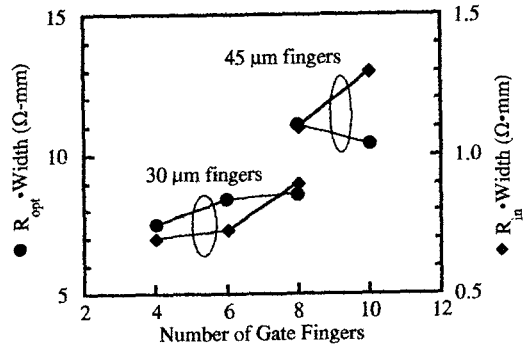

Fig. 4 Plot of measured normalized R_{opt} and extrinsic input resistance, R_{in}, versus number of fingers for a 0.25 μm PMODFET with V_{ds} of 2 V and I_{ds} of 60 mA/mm.

Simulation of MMIC noise figure is needed not only for low-noise amplifiers, but for MMICs with other design goals (e.g., broadband gain, or low DC power consumption, etc.). Therefore, a bias dependent noise model is useful for MMIC design. A bias dependent noise model was developed by making T_d a function of I_{ds} and V_{ds} [8, 10]. A comparison of the measured and modeled F_{min} and G_a at 12 GHz versus I_{ds}/width is shown in Fig. 5. The bias-dependent linear FET circuit model is similar to the HP Root non-linear FET model in that it is directly constructed from automatically characterized device data [11]. The usefulness of the bias-dependent scalable noise model was demonstrated with the simulation of a 0.5 to 50 GHz distributed amplifier that employs cascoded MODFETs [3]. There was good agreement between measured and simulated noise figures up to 50 GHz [3].

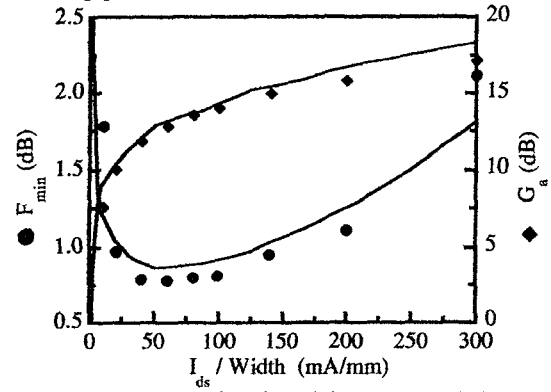

Fig. 5. Plot of measured and modeled F_{min} and G_a at 12 GHz versus I_{ds}/Width for a 180 μm wide, PMODFET with V_{ds} of 2 V.

IV. AMPLIFIER DESIGN

The noise model was used to design a three-stage 12 GHz low-noise MMIC amplifier. The design goals were lowest noise figure, more than 25 dB gain, small chip size, and input and output return loss less than -10 dB. Source inductance (negative feedback) was added to the PMODFET to improve the amplifier input return loss with little effect on F_{min}, but at the cost of gain. Source inductance was synthesized with a high impedance (9 μm wide) microstrip line. The tradeoff between gain and return loss was simulated by sweeping the length of the source line, as shown in Fig. 6. Return loss improves 2.9 dB per 1 dB loss of gain A transmission line length of 200 μm was chosen as a compromise for the 360 μm wide FET.

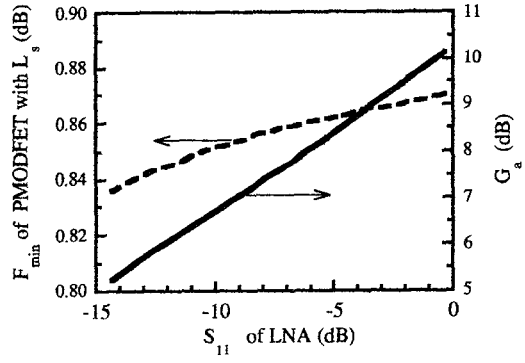

Fig. 6. Plot of G_a and F_{min} versus S_{11} for a 12 GHz ideal LNA. Parameters were changed by sweeping the length of a high impedance source line.

FET width is a useful design parameter for MMIC designers. The scalable device model was used to select a FET width for broad noise circles [12] and a simple input matching network (shunt inductance). Noise circles are

broader for a FET with a smaller $|\Gamma_{opt}|$ (i.e., angle of Γ_{opt} near 90°). The FET width was chosen so that Γ_{opt} lies on the 1/50 mho admittance circle. Then the input matching network was a simple shunt inductor. A simple matching network is preferred because it should be smaller and more likely correct. Fewer, smaller passive matching components are prefered because MMIC passive components are not high Q and degrade the noise figure of the LNA.

Small chip size, and single-supply non-tweaked bias are essential for MMICs in cost-competitive commercial markets such as DBS. Lumped components are necessary for small chips. The matching networks were designed with MIM capacitors and spiral inductors. The bias and matching networks were combined for size and simplicity, as shown in Fig. 7. The three-stage amplifier was made by cascading three identical stages. A photograph of the finished circuit is shown in Fig. 8.

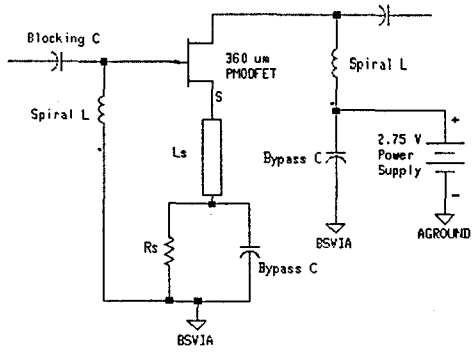

Fig. 7. Circuit schematic for a single stage of the 12 GHz LNA.

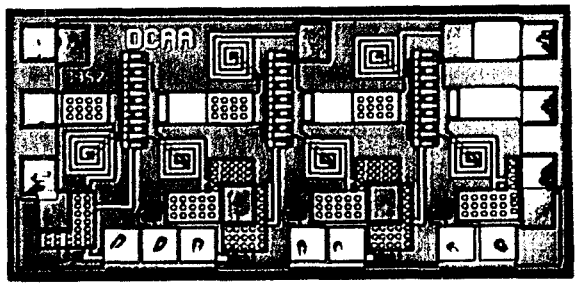

Fig. 8. Photograph of the three-stage 12 GHz MMIC LNA.

The I_{ds} for lowest F_{min} is small (60 mA/mm); therefore, it is very sensitive to V_p changes due to process variations (e.g., doping density and gate recess depth). Source resistance was incorporated in the design to reduce the sensitivity to V_p and thus enhance manufacturability of the LNA. The sensitivity was reduced by $1/(1+g_m \cdot R_s)$, which was a factor of 5 for this design. The LNA, with R_s, could tolerate a V_p variation of +/- 430 mV before the noise figure increased 0.1 dB. Biasing was reproducible; the standard deviation for drain current was 5.2 mA/mm (8%) for three wafers. The value of source resistor was selected so that the gate voltage was zero ($R_s \cdot I_{ds} = 0.78$) and hence the LNA needed only a single bias supply. R_s degrades the RF gain and increases thermal noise. To minimize these problems R_s was bypassed with a 6 pF capacitor, as shown in Fig. 7.

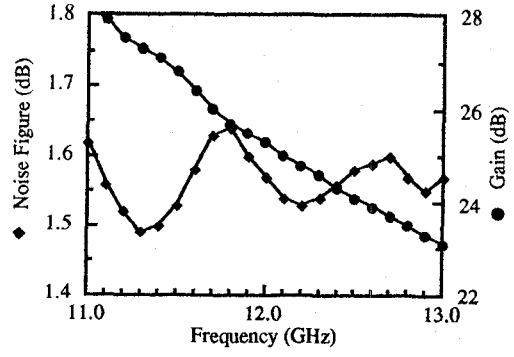

Fig. 9. Plot of measured noise figure and gain of LNA versus frequency.

V. Microwave Performance

The three-stage 12 GHz LNAs had a mean noise figure of 1.6 dB with a mean gain of 25.6 dB. The input and output matches were -13 dB and less than -25 dB, respectively. The frequency dependence of gain and noise figure are shown in Fig. 9. The standard deviations for three wafers for gain and noise figure were 0.5 dB and 0.08 dB, respectively. The small standard deviations are attributed to the reproducible biasing and the process parameter control. The best performance was a noise figure of 1.53 dB with 25.5 dB gain. The electrical yieldof the circuit was 91%. The noise figure, gain-per-stage, and return-loss are comparable or better than most 12 GHz MMIC LNAs, as shown in Table 1. The MMIC was biased with a single supply of 2.75 V drawing 73 mA.

VI. Discussion

The most remarkable feature is the MMIC size. The chip was only 0.92 mm^2 or 0.31 mm^2/stage. This chip size-per-stage is significantly smaller than previously reported 12 GHz MMIC LNAs. A comparison of 12 GHz MMIC LNAs is given in Table 1. The LNA reported here is less than half the size per gain stage of the previous smallest LNA.

Company	Ref.	Stages	F_{min} dB	F dB	G/stage dB	Area/stage mm^2/#
HP	-	3	0.86	1.6	8.2	0.31
Sharp	[20]	2	-	2.5	8.3	0.72
Sumitomo	[13]	4	0.7	1.1	6.5	1.20
Sumitomo	[14]	4	1.2	1.7	6.0	2.25
Hitachi	[15]	2	1.1	1.3	7.7	1.50
Matsushita	[16]	2	0.5	1.2	8.2	1.63
Mitsubishi	[17]	2	1.0	1.6	7.0	1.96
NEC	[18]	2	1.7	2.8	8.0	0.65
Toshiba	[19]	3	1.9	3.4	6.6	1.50

Table 1. Comparison of 12 GHz MMIC low-noise amplifiers.

The noise figure modeled for the LNA was 1.3 dB. A difference of 0.3 dB is not significant for most gain simulations, but important for noise figure. The 0.3 dB difference could be attributed to (1) coupling between components, (2) under estimate of passive component losses, (3) process variation, (4) measurement errors. The input return loss was better than modeled. This indicates that the input matching network was not optimum for lowest noise figure. The compact layout of the circuit results in un-modeled coupling between components. Coupling was probably a major cause of performance less than modeled.

VII. CONCLUSIONS

A scalable, bias-dependent FET noise model was developed for MMIC design. The FET noise model is based on the resistor temperature noise model of Pospieszalski. The noise temperature of the output resistor was made a function of I_{ds} and V_{ds} in a measurement based bias-dependent linear circuit model. All four noise parameters were modeled for PMODFETs of different widths, numbers of fingers, and biases.

A three-stage 12 GHz, MMIC low-noise amplifier was designed with the noise model. The LNA has a 1.6 dB noise figure and 25.6 dB gain. An RF bypassed source resistor was employed for biasing with a single power supply and for improved tolerance of process variations. Source inductance was added to obtain both low noise figure and acceptable input match. The FET width was chosen for broad noise circles and a simple input matching network. The LNA chip was designed significantly smaller per stage (0.31 mm^2/#) than previous MMIC LNAs by using lumped elements such as spiral inductors.

VIII. ACKNOWLEDGMENT

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